REMARKS

Applicants wish to thank Examiner Jones for the courtesy of the telephone interview with applicants' undersigned attorney on Thursday, October 2, 2003. In that interview, the present amendment was broadly discussed, but no agreement was reached regarding allowability of the claims.

Reconsideration of the rejected claims in view of this amendment is respectfully asked.

Claims 1-36 are finally rejected under 35 U.S.C. § 102 as being anticipated by Wells, of record. Wells discloses a system of a plurality of gaming devices 22 (which the examiner reads on the claimed "local controllers" or "nodes") interconnected with a gaming gateway 24 (which the examiner reads on the claimed "host controller") in a loop configuration (see Fig. 2). In other words, there are a string of the devices 22, with the devices at each end of the string, both being directly connected to the gateway 24, so that communication can proceed in either direction around the loop.

Applicants' claimed invention, on the other hand, is directed to a string arrangement with plural local controllers or nodes connected together in a string with a node at only one end of the string being directly connected to the host controller (see Fig. 1). In order to emphasize this fundamental distinction, claim 1 has been amended to specify that the controllers are interconnected in a string "such that only one local controller is directly connected to the host controller." Each of claims 13, 24 and 31 has been amended to recite a plurality of devices arranged in a string "having first and second spaced ends," and a host controller "directly connected to only the first end of the string." No such arrangement is disclosed or suggested by Wells and, therefore, for this reason alone, it is submitted that each of the independent claims 1, 13, 24 and 31 and the claims dependent thereon patentably distinguishes from Wells.

Additionally, claim 1 requires that each local controller or node have, in addition to a data in terminal, a data out terminal, a power terminal and a common terminal, "plural device terminals," which are "respectively connected to individual ones of the devices" to be individually accessed. Similarly, each of claims 13 and 24 requires that each local controller have plural "device output terminals to which the devices of the associated node may respectively be connected." Claim 31 has been amended to recite that each node includes plural devices "respectively connected to device terminals of" the local controller of the node. There is nothing in any of the gaming devices 22 of Wells corresponding to the claimed "device terminals" to which individual devices to be accessed may be respectively connected, nor does the examiner contend otherwise. Accordingly, this affords an additional basis for the allowance of claims 1-36.

Additionally, claim 1 recites a power line interconnecting the power terminals of the host controller and all the local controllers, and a common line interconnecting the common terminals of the host controller and all of the local controllers. No such arrangement is disclosed or suggested by Wells. The examiner contends that "One would also agree that the [Wells] system can be powered via a series circuit." But the issue is not how the Wells system might alternatively be configured. The rejection is under § 102. Thus the issue is whether or not the claim limitations are disclosed by Wells, and they are not. Wells does not disclose how the devices 22 are powered, but they certainly can be powered independently of one another and, indeed, that is likely to be the case if they are disposed remotely from one another. Thus, this affords an additional reason for the allowance of claim 1 and the claims dependent thereon.

Each of claims 13, 24 and 31 requires that each local controller include an M-bit shift register," with the nodes of the string being interconnected so that they cooperate to provide an

"(M x N)-bit shift register." Again, no such arrangement is disclosed or suggested by Wells. The examiner contends that "'bit shift registers' have been known since the birth of computers." Again, this is beside the point. The issue is what Wells discloses. The examiner further contends that Fig. 2 of Wells defines a 4 x 1-bit shift register "with gaming device (22) being M and gaming device (24) being N." Assuming, *arguendo*, that this were true, it does not meet the claim limitations. The claims require that both "M and N are whole numbers greater than one." More importantly, there is simply no discussion anywhere in Wells of shift registers, let alone an arrangement of local controllers such that shift registers in each of the controllers cooperate with one another to form a single shift register. Thus, this affords an additional reason for the allowance of claims 13, 24 and 31 and the claims dependent thereon.

The examiner comments that "applicant acquiesces to the rejection to claims 1-36" regarding the IEEE standard "by simply failing to reply to the rejection." But the examiner has not stated a separate ground of rejection based on the IEEE standard. The only rejection is a § 102 rejection based on Wells.

For all the foregoing reasons, it is respectfully submitted that, as amended, each of claims 1-36 is now in condition for allowance and the allowance thereof is respectfully asked.

Respectfully submitted,

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